Pci local bus specification revision 2.2 pdf

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By ExtremeTech Staff on September 21, 2001 at 2:24 pm This site may earn affiliate commissions from the links on this page. Terms of use. Controlling the power state of the PCI bus lets a system control peripherals and support Wake events. The original PCI spec ignored power management; this spec implements it. The PCI Power Management Spec requires the operating system to track the bus's power state, including whether a system is busy or idle. It recognizes four power states each for the bus and for peripherals (power on, power off, and two intermediate-power states). Using this information, the system can manage power along the bus, including that for different peripherals and for Wake events. This white paper describes the new spec in both prose and complementary graphics, tables, and engineering diagrams. PCI Bus Peripheral Component Interface [PCI Bus Description] [PCI Interface ICs] [PCI Connectors] [PCI Bus Pinout] [PCI Standard] [PCI Size] [PCI COTS Cards] [PCI Chassis Manufacturers] [Home] A Brief Description of the Peripheral Component Interface 'PCI' Bus The Peripheral Component Interface 'PCI' Bus was originally developed as a local bus expansion for the PC (ISA) bus, and was coined the PCI Local Bus. The spec started as an add-on to the ISA form factor with the PCI requiring its own connectors. The PCI spec defines the Electrical requirements for the interface. No bus terminations are specified, the bus relies on signal reflection to achieve level threshold. The first version of the PCI bus ran at 33MHz with a 32 bit bus (133MBps), the current version runs at 66MHz with a 64 bit bus. The PCI bus operates either synchronously or asynchronously with the "mother Board bus rate. While operating asynchronously the bus will operate at any frequency from 66MHz down to (and including) 0Hz. Flow control is added to allow the bus to operate with slower devices on the bus, allowing the bus to operate at their speed. PCI is an unterminated bus, the signal relay on signal reflections to attain there final value. The PCI specification has been port-ed to a number of other form factors. These include: PCI: The original specification 'Peripheral Component Interface', @ Rev 2.2 PCI-X: The latest version 64 bits at 133MHz cPCI, Compact PCI: PCI in a VME form factor, 3U/6U using 2mm connectors PC104-Plus: PCI add-on to the PC104 spec, ISA in a square form factor PISA: PCI add-on with PCAT to the ISA AT form factor P2CI: PCI on the VME64 P2 connector PMC: PCI on a Mezzanine Card, 'PMC' PXI: cPCI for Instrumentation IPCI: Industrial PCI (Another version of cPCI} Serial PCI PCI on a serial link Card Bus: 32 bit PCI on the PC Card (PCMCIA) Format Each of these additional specifications rely on the PCI spec., normally only the mechanical (form factor) definition changes. Unlike earlier PC buses, the PCI bus is processor independent. The (64bit) PCI bus is made up of the following (major) signals: Address/Data Bus: 64bit Address; 64bit Data, Time Multiplexed System Bus: 2bits; Clock/Reset Interface Control Bus: 7bits; Ready, Acknowledge, Stop. Parity Bus: 2 bits, 1 for the 32 LSBs and 1 for the 32 MSB bits Errors Bus: 2 bits, 1 for Parity and 1 for System Command/Byte Enable: 8 bits (0-3 @ 32bit, and 4-7@ 64bit Bus) 64MHz Control: 6 bits; (2) Enable/Running, (2) Present, (2) Ack/Req Cache: 2 Bits Interrupt bus: 4 bits JTAG Bus: 5 bits Power: +5, +3.3, +12, -12v, GND The Time Multiplexed Address and Data bus may exist as either 0 to 31 bits (32bits) or 0 to 63 bits (64bits) using the 64 bit expansion bus. Both the Address and Data line use the same bus, Address first then Data. 32 bit PCI may also use 64 bit addressing by using two address cycles; termed Dual Address Cycles (DAC), the low order address is sent first. Additional control bits are utilized once the bus is increased to 64 bits. The specification defines both a Reset line and a Clock line. The Clock may be either 33MHz or 66MHz. I believe the 66MHz clock rate is only defined for the 64bit bus width. See PCI Bandwidth, below. A number of 'Handshake' lines exist to allow communication, i.e. Ready, and Acknowledge Two Parity lines are made available, one for the 32 bit bus width (bits 0 to 31) and an additional one for the 64 bit expansion (bits 32 to 63). Two error bits; I assume, 1 for the LSB 32 bits and one for the upper 32 bits. PCI cards for a personal computer differ from the ISA type by two important factors: Components are mounted on the reverse side of the card & the edge connector is more dense, shorter and the keys reside in different locations The PCI bus uses either 32 or 64 bits of parallel data, depending on the version. So with each clock tick, 32 or 64 bit data is transferred over the bus. Transferring 64 bits at a time translates to a very large parallel bus, using a minimum of 64 lines in addition to all the required control and signal lines. A new version of the PCI bus has been released using a differential serial bus instead of a parallel bus [Parallel PCI]. The upgrade path for PCI would be PCI-X for higher speed operation. However if compatibility is not required, PCIe would be the preferred alternative. The new serial PCI Bus is called the PCI Express Bus: while the version discussed on this page is now referred to as Conventional PCI. The PCI Express bus offers a reduced cost solution because the PCI Express Bus only requires a few sets of differential lines freeing up board space and requiring a smaller connector. The motherboards appearing in 2004 began to have a PCI Express bus instead of an AGPnote 1 slot connector, and one or two PCI Express slots next to the remaining Parallel PCI bus slots. Over the next few years the PCI Express bus will replace the Parallel PCI bus slots on a MotherBoard because of its reduced cost and high bus speed. The PCI Express bus is not compatible with the standard PCI bus. The PCI Express connectors, signal voltage levels, and signal format are different then with PCI. However; the physical size of PCI Express cards has the same dimensions as standard PCI cards. The main physical difference between the two bus formats lay with the connectors, the main electrical difference is a differential serial bus instead of a single ended parallel bus. The point here is that although Parallel PCI is not yet obsolete, there is a state-of-the-art replacement in PCI Express. Keeping in mind that Parallel PCI will be around for years to come just as the ISA bus is still around. Note 1 Recall the AGP bus was derived from the PCI bus. The PCI bus doesn't use Glue logic, being developed as a single chip interface bus. So signal chip solutions or ASIC parts are the only PCI chips listed below. PCI is a CMOS bus, with no current flowing in the static state. The +5 volt interface uses standard TTL switching levels; VIH = 2v, VOH = 2.4v. The +3.3 volt interface uses VIH = 1.65v, VOH = 2.97v Integrated Circuit Vendors; Altera {PCI Cores} Analog Devices {ISA-PCI Interface Bus ICs} Conexant {PCI video decoders} Cirrus Logic {PCI-Disk Controllers} Cypress Products Dolphin Interconnect LLC {PCI to StarFabric Bridge} Eureka Technology, Inc {PCI Host Bridge, AHB-PCI Host Bridge, PCI-PCI Bridge, PCI-ISA Bridge, PCI Bus Arbiter} IDT {PCI to StarFabric Bridge} Infineon Technologies {PC Chips-DRAM Controller ICs} Intel Marvell {PCI chip set Manufacturer} PLX Technology Inc. {PCI to PCI Bridge ICs} QLogic {PCI-SBus Interface Bus ICs} QuickLogic {PCI Controller} Texas Instruments 'TI' {Bridges-Controller IC Manufacturer} Xilinx {FPGA Core 32-bit PCI system running at speeds up to 66 MHz} IC Chip Manufacturers {All other functions and interfaces} Note that support for IC semiconductors will continue to fall as the interface becomes older. No new semiconductors will be developed for such an out-dated interface. {PCI Bus Index} PCI Bus Online Standards and Specifications PCI Local Bus Specification: PCI version 1.0 was developed by Intel in 1991 but not released by a Standards body. PCI revision 2.0; released in 1993; 32-bit, 33MHz bus. PCI revision 2.1; released in 1995; 32-bit, 33MHz / 64-bit, 66MHz, Universal PCI for 3.3v or 5v cards PCI revision 2.2; released 1998; minor clarifications / enhancements. PCI revision 2.3; released in 2002; removed 5v only cards PCI revision 3.0; released in 20xx; removed 5 volt interfaces altogether. PCI Standards Body: PCISIG: Peripheral Component Interconnect - Special Interest Group [www.pcisig.com] PICMG [www.picmg.org] {PCI Industrial Computer Manufacturers Group} PCI in other Form Factors: PCI: The original specification 'Peripheral Component Interface', @ Rev 2.1 PCI-X: The latest version 64 bits at: PCI-X 66, PCI-X 133, PCI-X 266 and PCI-X 533 [4.3GBps] cPCI, Compact PCI: PCI in a VME form factor, 3U/6U using 2mm connectors Mini PCI: PCI in a small form factor for Laptops, 59.75 mm x 50.95 mm x 5mm. 32 bit data bus running at 3.3v PC104-Plus: PCI add-on to the PC104 spec, ISA in a square form factor PCI/104: PCI only to the PC104 spec, removing the PC XT and AT buses from the PC/104 specification PISA: PCI add-on with PCAT in the ISA AT form factor P2CI: PCI on the VME64 P2 connector PMC: PCI on a embedded Mezzanine Card, 'PMC' PXI cPCI for Instrumentation IPCI: Industrial PCI (Another version of cPCI} Serial PCI: PCI on a serial link Card Bus: 32 bit PCI on the PC Card (PCMCIA) Format PCI Express Bus: PCI over a differential serial link. The PCI Express physical layer is not compatible with the PCI bus listed on this page Mini PCI Express Bus: PCI over a differential serial link in a small form factor for Laptops. The PCI Express physical layer is not compatible with the PCI bus listed on this page Note: the PCI bus has been ported to a number of different embedded or industrial card form factors, many different board types are listed above. How ever; this page may be missing some. Use the Buses icon at the bottom of the page to search for a particular embedded board form factor or bus type. Other PCI form factor bus pages may contain additional data or pin outs. Some buses use the PCI bus specification out-right, others change the form factor. Some specifications use a reduced pin-out, while others only use the minimum bus width of 32 bits ~ all PCI based. Keep in mind the PCI Express bus discussed above remains software compatible with the older Parallel PCI bus, but is not electrical or physically compatible. Common PCI Bus Questions: Can I use a PCI card in a PCI Express card slot; No the electrical and physical interfaces are completely different. Can I use a PCI Express card in a PCI card slot; No electrical and physical interfaces are completely different. Can I make a dongle to convert PCI card in a PCI Express card slot; No not with out a major design effort. Is the PCI Express card pinout the same as a PCI card pinout; No, the slot pin outs are completely different. Is the PCI Express card slot faster than a PCI card slot; Yes, see the PCI Express page. I'm an over-clocker, do I need a Parallel PCI slot, No it's older technology operating at a reduced speed. Can I convert a PCI card into a PCI Express card slot; No, Not really, with out a major engineering effort. Can I purchase a converter which translates a PCI card into a PCI Express card slot; Yes. Why would I want a Parallel PCI bus slot; to use older PC cards currently still being produced in the market place. Should I purchase a mother board with an older PCI slot; it depends on if you want to add a card which is not yet produce using PCI Express. So, if your a high-end user, or PC Over-Clocker, you want PCI EXpress, or a computer at the lowest value and don't plain to add a card, you want PCI. What is PCI; an expansion bus for personal Computers used at add cards and features to a PC mother board. PCI Board Size PCI Local Bus implementations will support up to four add-in card connectors, although expansion capability is not required to support daughter boards. Four sizes of PCI add-in cards are defined: long, short, Low Profile, and variable short length. The long add-in cards include an extender to support the end of the add-in card. To accommodate the 3.3V and 5V signaling environments and to facilitate a smooth migration path between the voltages, two add-in card electrical types are specified: a "universal" add-in card which plugs into both 3.3V and 5V connectors and a "3.3 volt" add-in card which plugs into only the 3.3V connector. PCI Card PCI card dimensions Full/Half Size 3.3 volt Card Detailed Dimensions The standard PCI Form factor is 106.68mm x 312mm [4.2" x 12.28"] PC PCI card dimensions Half Size Detailed w/ PCI and ISA Bus Pinout The standard PCI Form factor is 107mm x 312mm [4.2" x 12.28"] PC PCI Pinout 32/64 bit cards. PCI Signal Assignments. Signal Descriptions and signal names are also provided on the pin-out page. Designer note; the pinout provided on the pin-out pages relates to the PCI main board connector on the mother board. Add-in cards [daughter boards] may have a slightly different connector pin out. {PCI Bus Index} PCI Bus Connector Manufacturers A PCI connector accepts a card edge. The PCI connector will have one or two keys [plastic gaps] in the connector. One key-Way indicates 3.3 volt operation [instead of 5 volt operation], and the other Key-Way indicates 64-bit operation. A 32 bit card would only have one key at most to indicate 3.3 volt operation. Refer to the PCI Pin Out page for the location of the Key-Ways. Laptops/NoteBooks which use the Mini PCI standard [link above] use a different type of connector. Only manufacturers producing connectors for the Desk Top Personal Computer PCI Bus are listed below. Refer to the other pages listed above to find connector manufacturers of the other types of embedded PCI buses. 32-bit 5V: Connectors with the notch farthest from the backplate 32-bit 3.3V: Connectors with the notch closest to the backplate 32-bit Universal PCI: Connectors with notches in both the 5V and 3.3V positions 64-bit 5V: 32-bit 5V PCI connectors, two key ways off-set right of center 64-bit 3.3V: 32-bit 3.3V PCI connector, one key far left, one just center right 64-bit Universal PCI: 32-bit Universal PCI connector, one key far left, two key ways off-set right of center PCI Connector Dimensions AVX {PCI connector Manufacturer} FCI Meritec {5v/3.3v angled PCI Connectors, PCI Cable Assemblies} Tyco Electronics {Back to Peripheral Component Interface Bus [PCI] Index} PCI Bandwidth There are a number of possible PCI bus speeds based on the clock rate. These are peak transfer rates, which translate to interface bandwidth. 132 MB/s using a 64-bit data path at a 33 MHz clock rate. 264 MB/s peak using a 32-bit data path at 66 MHz 264 MB/s peak using a 64-bit data path at 66 MHz 532 MB/s peak using a 32-bit data path at 133 MHz 1064 MB/s peak using a 64-bit data path at 133 MHz Although PCI was never really used as a video interface, because AGP was introduced. This link provides a through-put graph of the different video interfaces; Bandwidth comparison of different video expansion buses, PCI included. As with any speed rating; a capital M means Mega, and a capital B stands for Bytes. Modified 7/16/2015 © 1998 - 2016 All rights reserved Larry Davis

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